REMARKS

In response to the Advisory Action mailed January 23, 2008, Applicants respectfully request reconsideration and entry of this amendment. Claims 1 and 3-30 were previously pending in this application. By this amendment, claims 1, 3, 5, 8, 9, 11, 13, 14, 24-26, 29 and 30 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26, and 30 being independent. No new matter has been added.

Summary of the Examiner Interview

As a preliminary matter, Applicants' representatives thank Examiner Hassan for granting and conducting a telephone interview on September 10, 2008. The substance of the telephone interview is summarized below in responding to the outstanding rejections of the claims.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 26, 27 and 30 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

During the telephone interview, the Examiner indicated that the claim amendments overcame this rejection.

Rejections Under 35 U.S.C. §103

I. The Office Action rejected claims 1, 3-9 and 13-25 (including independent claims 1 and 24) under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis et al. (U.S. Patent No. 5,797,043), hereinafter "Lewis," in view of George et al. (U.S. Patent No. 6,785,829), hereinafter "George." Applicants respectfully disagree. Independent claims 1 and 24 have been amended to recite, inter alia, that the stream register unit is configured to, when the FIFO coupled to the peripheral provides, in response to a request for data from the stream register unit, an indication that the data is not available, *send a stall signal to the execution unit*, causing the execution unit to stop executing instructions (emphasis added). None of the cited references teaches or suggests this limitation.

On pages 9 and 10, while rejecting dependent claims 10 and 11, the Office Action concedes that Lewis and George do not teach "wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the execution unit, causing the processor to stop executing instructions." The Office Action then alleges that Lai[1] teaches this limitation as "issue a stop signal, column 3, lines 20-26." Applicants respectfully disagree.

Lai is directed to delayed transaction method and system to handle multiple delayed transactions in a PCI system (Abstract). Lai discusses that, when the initiator 30 asserts FRAME signal and sends out address and command on the PCI bus 34, a stop signal STOP is asserted if the target, i.e., the responder 32, is not ready to transfer data to the initiator 32 (col. 5, lines 4-7; Fig. 3). With reference to Fig. 4, Lai discusses that in cycles T5 and T12 , STOP is asserted by the responder 32 , so that FRAME is deasserted in cycles T6 and T13 corresponding to function units 36a and 36b, respectively (col. 6, lines 23-25). The initiator 30a deasserts request signal REQ1 in cycles T6 and T13 (col. 6, lines 26-27). Thus, the STOP signal of Lai is different from a stall signal sent to the execution unit recited in claims 1 and 24. In Lai, the STOP signal is asserted by a responder to deassert a FRAME signal sent by an initiator to the responder. For example, Lai discusses that, *when data transfer to the function unit 36a is completed*, the initiator 30a, *issues a stop signal STOP* in cycle T25, indicating that the data transaction is completed (col. 6, lines 47-49) (emphasis added). Thus, FRAME and TRDY are deasserted in cycle T26, and IRDY is deaserted in cycle T27 (col. 6, lines 49-51. In contrast, each of independent claims 1 and 24 recites that the stream register unit is configured to, when the FIFO coupled to the peripheral provides, in response to a request for data from the stream register unit, an indication that the data is not available, send a stall signal to the execution unit, *causing the execution unit to stop executing instructions* (emphasis added). Therefore, Lai does not teach or suggest this limitation.

In view of the foregoing, claims 1 and 24 patentably distinguish over Lewis, George and Lai, either alone or in combination.

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[1] On page 9, the Office Action includes an incorrect number for a U.S. Patent of Lai. During a phone call on September 29, 2008, the Examiner indicated that the correct number for Lai is U.S. Patent No. 6,549,964.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-25 is respectfully requested.

II. The Office Action rejected claims 26-30 (including independent claims 26 and 30) under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis in view of Garcia et al. (U.S. Patent No. 6,433,785), hereinafter "Garcia."

On page 12, the Office Action concedes that Lewis "fails to teach a register wherein if the data item being requested is not available, sending a timeout signal to the processor." The Office Action then states that Garcia "teaches a register wherein if the data item being requested is not available, sending a timeout signal to the execution unit of the processor (timeout counter, column 5, lines 26-42)." However, Garcia discusses that, in one embodiment, the timeout counter 124 counts six periods of a host bus clock before expiring (col. 4, lines 6-7). Other embodiments of Garcia may use other clock signals as a reference, or may count different numbers of clock periods before expiring (Garcia, col. 4, lines 7-9). As a result of the assertion of the second request pending signal 320 and the continued non-assertion of the posted write buffer available signal 350, the timeout counter 124 is initiated with a count of 6 at time C (Garcia, Fig. 3; col. 5, lines 29-33). The timeout counter 124 begins counting down from time C until the posted write buffer available signal 350 is asserted at time D, indicating that the posted write buffer 126 is available to receive the data associated with the first postable write transaction request (Garcia, Fig. 3; col. 5, lines 33-37).

Thus, the timeout **counter** of Garcia **counts down** until the posted write buffer becomes available for the second transaction (emphasis added). In contrast, claims 26 and 30 recite sending a timeout **signal** to the execution unit of the processor **causing the processor to interrupt** such that it can execute tasks other than the request (emphasis added). Therefore, the timeout counter of Garcia is different from timeout signal recited in claims 26 and 30. In view of the above, contrary to the assertions made in the Office Action, Garcia does not teach or suggest sending a timeout signal to the execution unit, as recited in each of claims 26 and 30.

Moreover, claim 26 recites, inter alia, that the stream register is arranged to... when the requested data item is not in the at least one FIFO, *send a stall signal* to the execution unit of the processor; and ... when the data item is not available and *when the stall signal has been active for a predetermined amount of time*, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request (emphasis added). Similarly, claim 30 recites, inter alia, that the stream register is arranged to... when the requested data item is not in the at least one FIFO, *send a stall signa*l to the execution unit of the processor; and ... when the data item is not available and *when the stall signal has been active for a predetermined amount of time*, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request (emphasis added). The Office Action does not address these limitations of claims 26 and 30.

None of the cited references teaches or suggests the above limitations. As discussed above, Lewis, George and Lai do not teach or suggest these limitations. Garcia discusses that, if the posted write buffer is unavailable when a postable write transaction request is received by the memory controller, the memory controller *stalls the host bus* and waits for the posted write buffer to become available (col. 3, 53-57). Thus, Garcia describes stalling the host bus rather than sending a stall signal to the execution unit of the processor, as recited in each of independent claims 26 and 30. Therefore, Garcia does not teach or suggest that the stream register is arranged to...send a stall signal to the execution unit of the processor; and ... when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request, as recited in claims 26 and 30.

In view of the foregoing, claims 26 and 30 patentably distinguish over Lewis and Garcia, either alone or in combination.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-30 is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

By: _____

James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000